Faster, Thinner, and more Complex … - Can this be Achieved?

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***Abstract*— Introduction of a novel low loss bondply for HDI multilayer printed circuit boards and high speed flex cables**

***Keywords*— low loss bondply, HDI multilayer, high speed flex cables, rigid flex multilayer, via fill**

I. Introduction

Are you designing high speed flex cables, mostly as rigid-flex multilayer pcbs? (Fig. 1) Aren't you losing your sleep over whether your design can actually get accomplished, which includes whether a pcb shop will actually be able to build such kind of pcbs?

Fig. 1. High speed rigid-flex cable

There is a solution for you: It's called EZPURE. This is a 1.5 and 3 mil (0.38 and 0.76 mm) thick non-reinforced thermoset resin bondply, which can get bonded in any multilayer press at 200 ºC for both, rigid and flex sections.

II. The Case For EZPURE

Why would a design engineer choose such a bondply? Well, the answer is simple: this homogenous isotropic material has a dielectric loss of 0.0032 at 10 GHz, and a DK of 2.8.

Although EZPURE does not contain any glass fabric, due to nanofiller technology a low Z_{CTE} of 44 ppm is achieved.

In addition it leads to consistently flat, level dielectric layers. (fig. 2, 3)

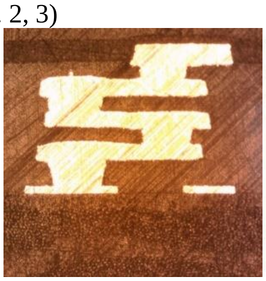

Fig. 2. Staggered Vias

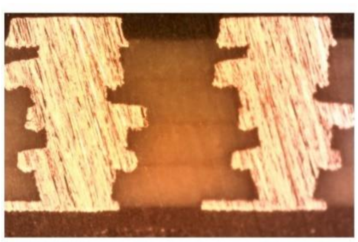

Fig. 3. Stacked Vias

Its homogeneous structure is suitable for good laser processability of HDI structures (Fig. 4).

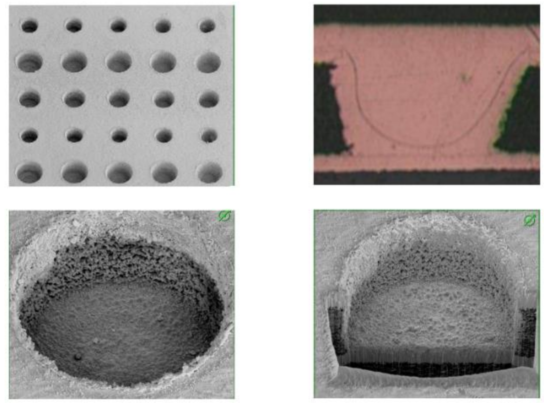

Fig. 4. Tests completed with ESI 5535 UV Nd:YAG nanosecond laser show good laser via quality

III. Reliability

During EZPURE's development cycle a 10 layer test vehicle was produced with 2, 3, and 4 stacked and staggered microvias to evaluate thermal reliability, which included 6 mil (0.15 mm) microvias and 4 mil (0.10 mm) dielectric spacing. Overall thickness was 0.065" (1.65 mm)

Thermal reliability of this composite rigid-flex multilayer pcb (EZPURE, Dupont Pyralux® AP and FR4) was demonstrated in passing of IST, HATS, and Lead Free Solder Reflow (table 1).

[redacted] Thermal Reliability				
Test Standard	Via Size	Preconditioning	Cycles	Pass/Fail
IST	17.5 mil and 17.7 mil (50 mil and 100mil pitch)	6X at 260°C	1000 Cycles Room Temp. to 160 °C	Passed (<10% Change in resistance)
HATS	7.9 mil, 9.8 mil, 14.5 mil and 17.7 mil	-	500 Cycles -55 °C to 125 °C 2 cycles per hour	Passed (<10% Change in resistance)
Solder Stress	-	6x at 288 °C	-	Passed
IPC-6013 Group A	-	-	-	Passed

Table 1. Thermal reliability of EZPURE

Also Signal Integrity testing was carried out. 50 Ω single-ended and 100 Ω differential lines were present in both stripline structures. Impedance measurements were all acceptable, as well as insertion loss (Table 2).

			Insertion Loss at 12 GHz		Insertion Loss at 24 GHz	
Description	Trace Width	Length	Loss (dB)	Loss (dB/in)	Loss (dB)	Loss (dB/in)
Layer 3 Differential	0.0055"	12"	7.656	0.638	14.160	1.180
Layer 3 Differential	0.0055"	24"	14.833	0.618	26.694	1.112
Layer 3 SE	0.0055"	12"	7.886	0.657	14.695	1.225
Layer 3 SE	0.0055"	24"	15.421	0.643	28.403	1.183
Layer 6 Differential	0.006"	12"	7.395	0.616	13.730	1.144
Layer 6 Differential	0.006"	24"	14.314	0.596	25.663	1.069
Layer 6 SE	0.00625"	12"	7.499	0.625	13.983	1.165
Layer 6 SE	0.00625"	24"	14.597	0.608	26.505	1.104

Table 2. EZPURE SI testing

For further reliability studies of stacked and staggered vias OM Thermal Stress System was carried out, a performance based reliability test methodology which performs air-to-air thermal shock per IPC TM-650 2.6.7.2., during which continuous 4-wire resistance is being monitored (Fig 5).

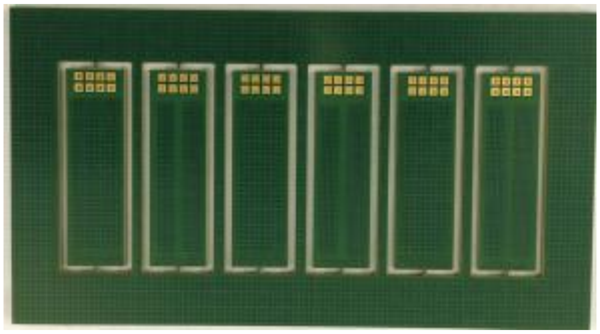

Fig. 5. IPC 2221B Appendix A type D-coupons for OM Thermal Stress System

6x reflow at 260°C and 100 cycles -55 to 178°C are excellent test criteria for assessment of long term reliability of a number of stacked vias in a design (Fig. 6 – 9).

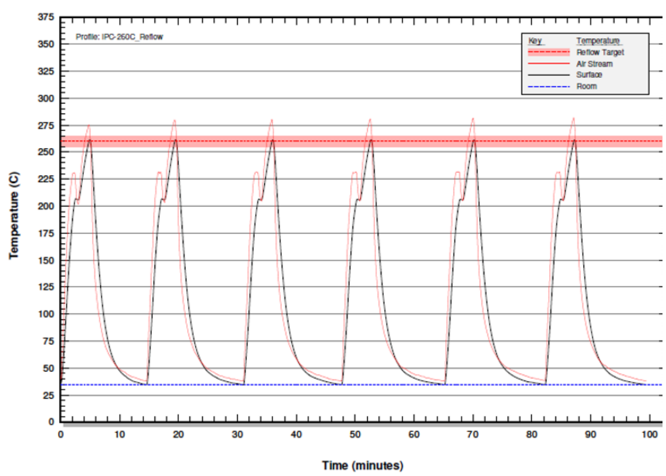

Fig. 6. Reflow Temperature Profile

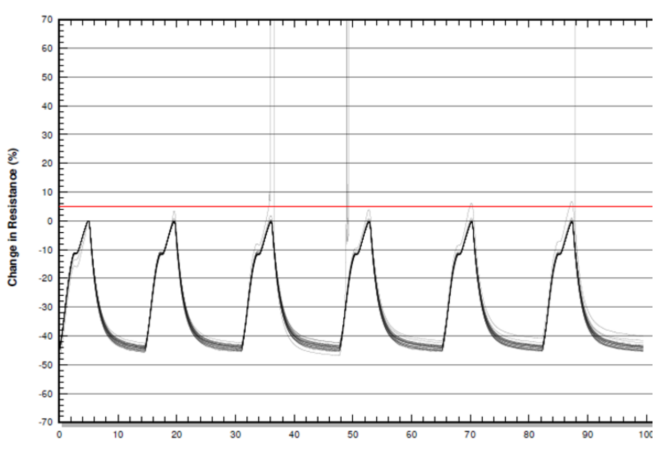

Fig. 7. Change in Resistance During Reflow

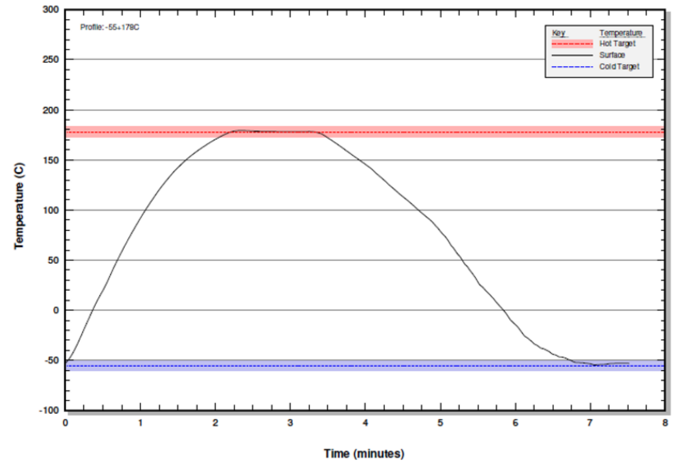

Fig. 8. Thermal Cycling Temperature Profile

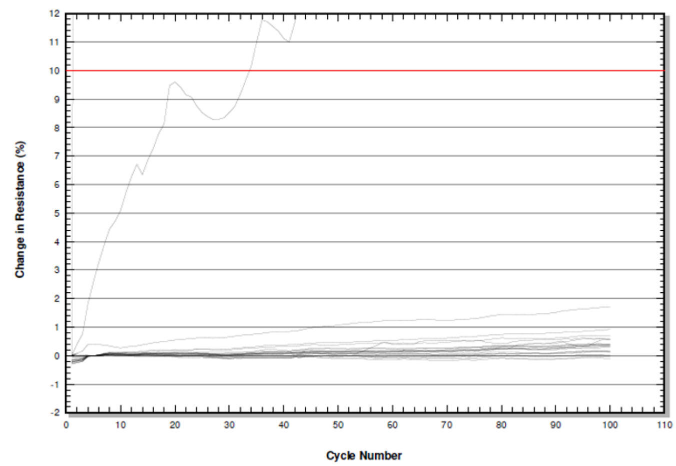

Fig. 9. Change in Resistance During 100x Thermal Cycling

Evaluations of all test coupons show that 2 and 3 stacked via configurations are possible (Table 3)

Material	**Stacked Via Configuration**		
	2	3	4
	Pass after 6x Reflow 260ºC		
EZpure-0055H	**12**	**12**	**10**
	Pass after 100 Thermal Cycles		
EZpure-0055H	**12**	**12**	**9**

Table 3. All 12 test coupons pass 2 and 3 stacks; 4 stacks are still a challenge

IV. Actual Designs

Fig. 10 and 11 show microsections of actual designs

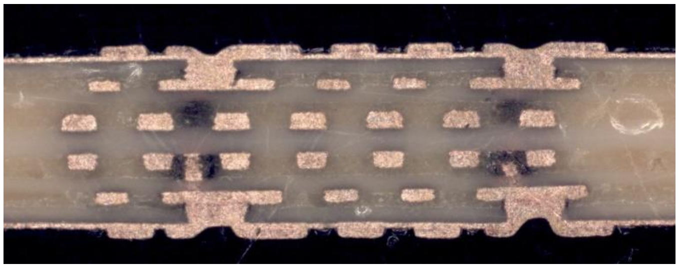

Fig. 10. 2-2-2 build-up using 2 mil EZPURE

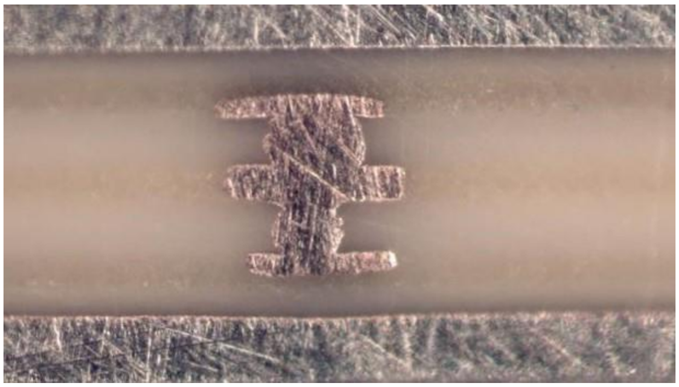

Fig. 11. EZpure

The isotropic nature of EZPURE also open up further new avenues in HDI designs. It's buried via fill capacity is unrivalled (Fig. 12).

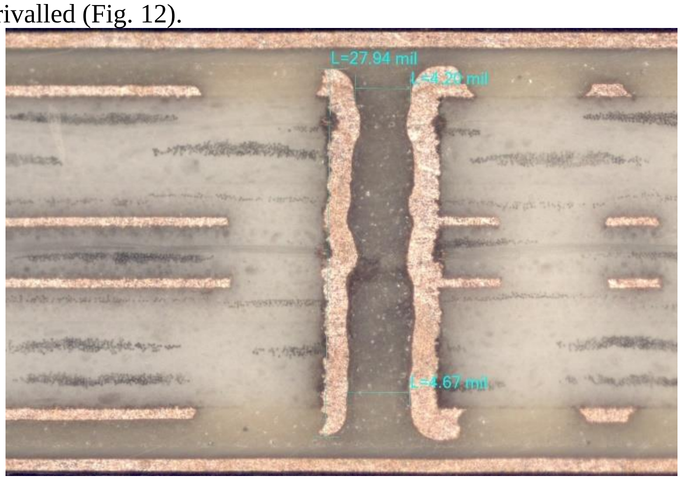

Fig. 12. Via Drill Size: 0.008" (0.2 mm), Buried Via Depth: .028" (0.71 mm)

V. Conclusion

EZPURE bondply leads the way for the most challenging HDI designs. Currently not many pcb fabricator are capable yet of manufacturing such type of printed circuit boards. However they now have in important tool for it.